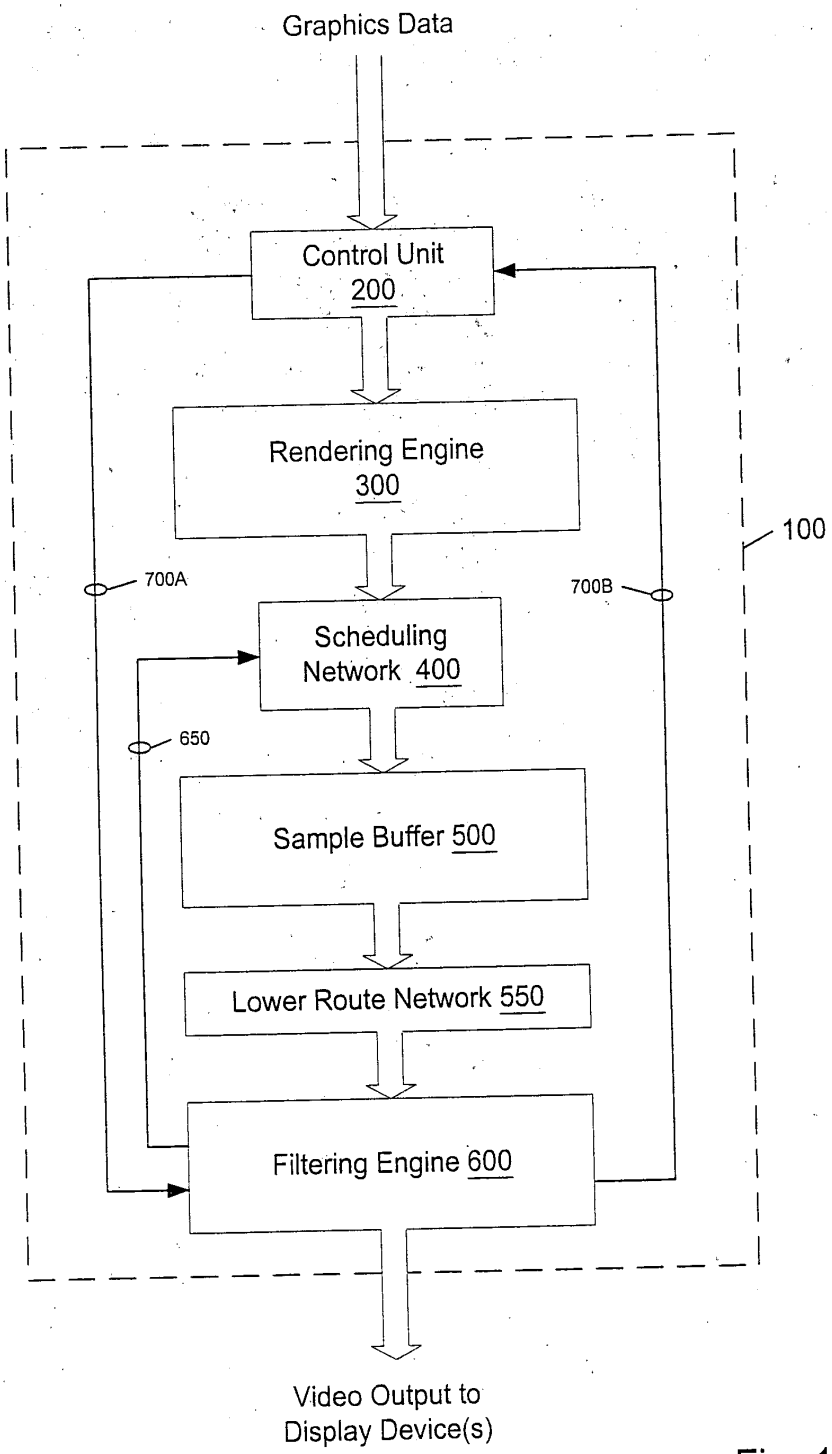

Graphics Data
Control Unit
200
Rendering Engine
300
100
700A
700B
Scheduling
Network 400
650
Sample Buffer 500
Lower Route Network 550
Filtering Engine 600
Video Output to
Display Device(s)

Fig. 1

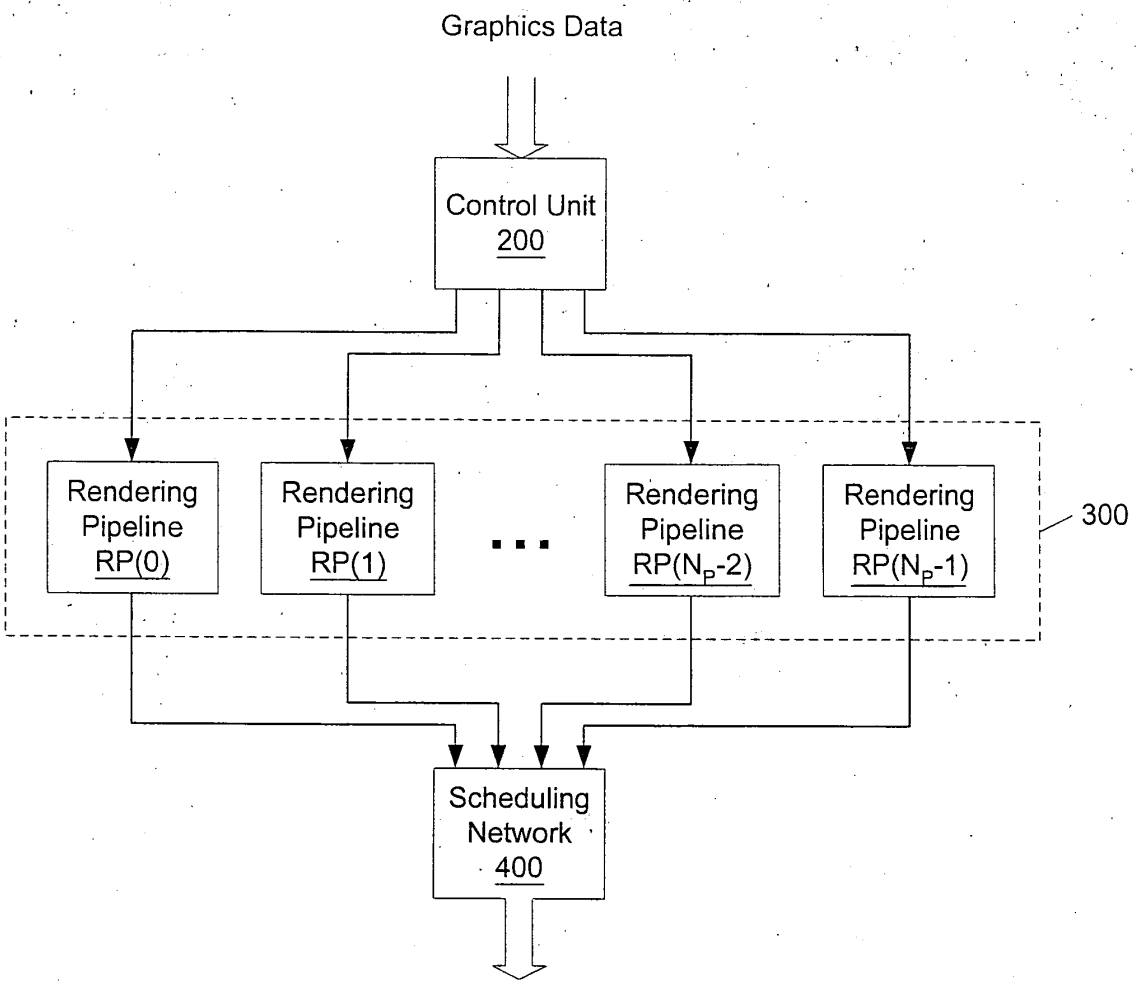
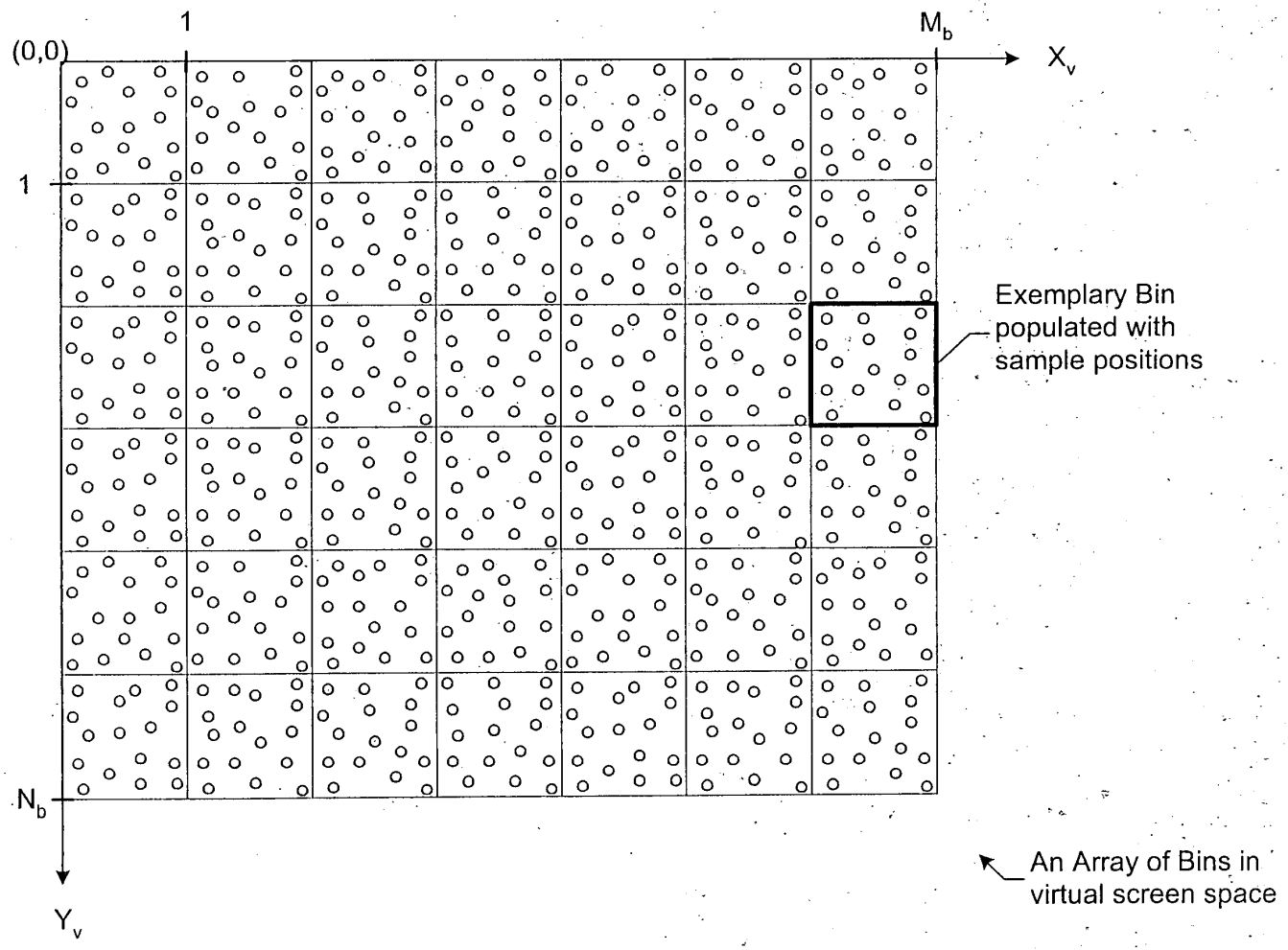

Graphics Data
Control Unit
200
Rendering
Pipeline
RP(0)
Rendering
Pipeline
RP(1)
Rendering
Pipeline
RP(N_P-2)
Rendering
Pipeline
RP(N_P-1)
300
Scheduling
Network
400
Sample Data to
Sample Buffer 500

Fig. 2

Fig. 3


(0,0)
1
1
M_b
X_v
N_b
Y_v
Exemplary Bin populated with sample positions
An Array of Bins in virtual screen space

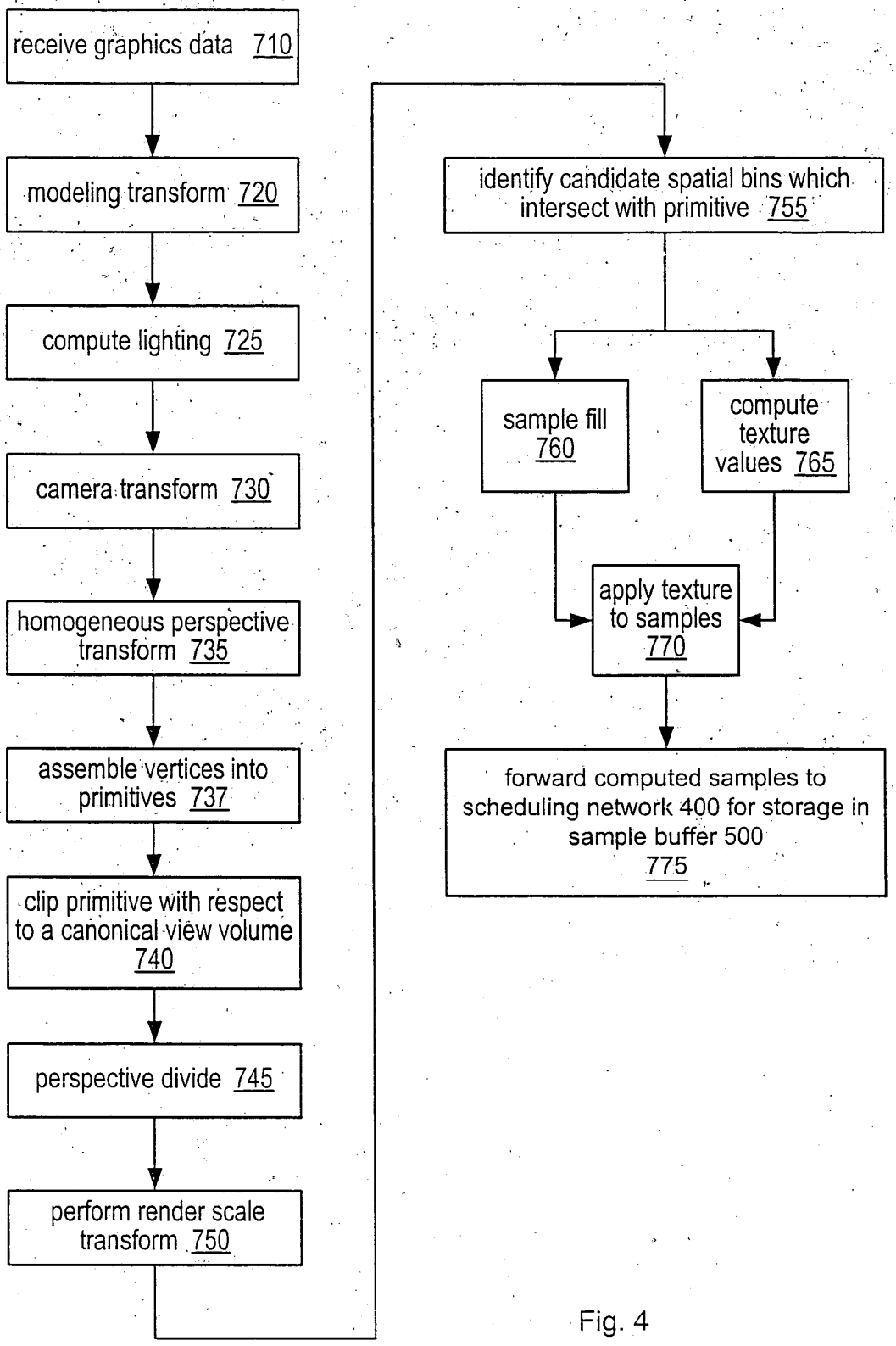

receive graphics data 710
modeling transform 720
compute lighting 725
camera transform 730
homogeneous perspective transform 735
assemble vertices into primitives 737
clip primitive with respect to a canonical view volume 740
perspective divide 745
perform render scale transform 750
identify candidate spatial bins which intersect with primitive 755
sample fill 760
compute texture values 765
apply texture to samples 770
forward computed samples to scheduling network 400 for storage in sample buffer 500 775

Fig. 4

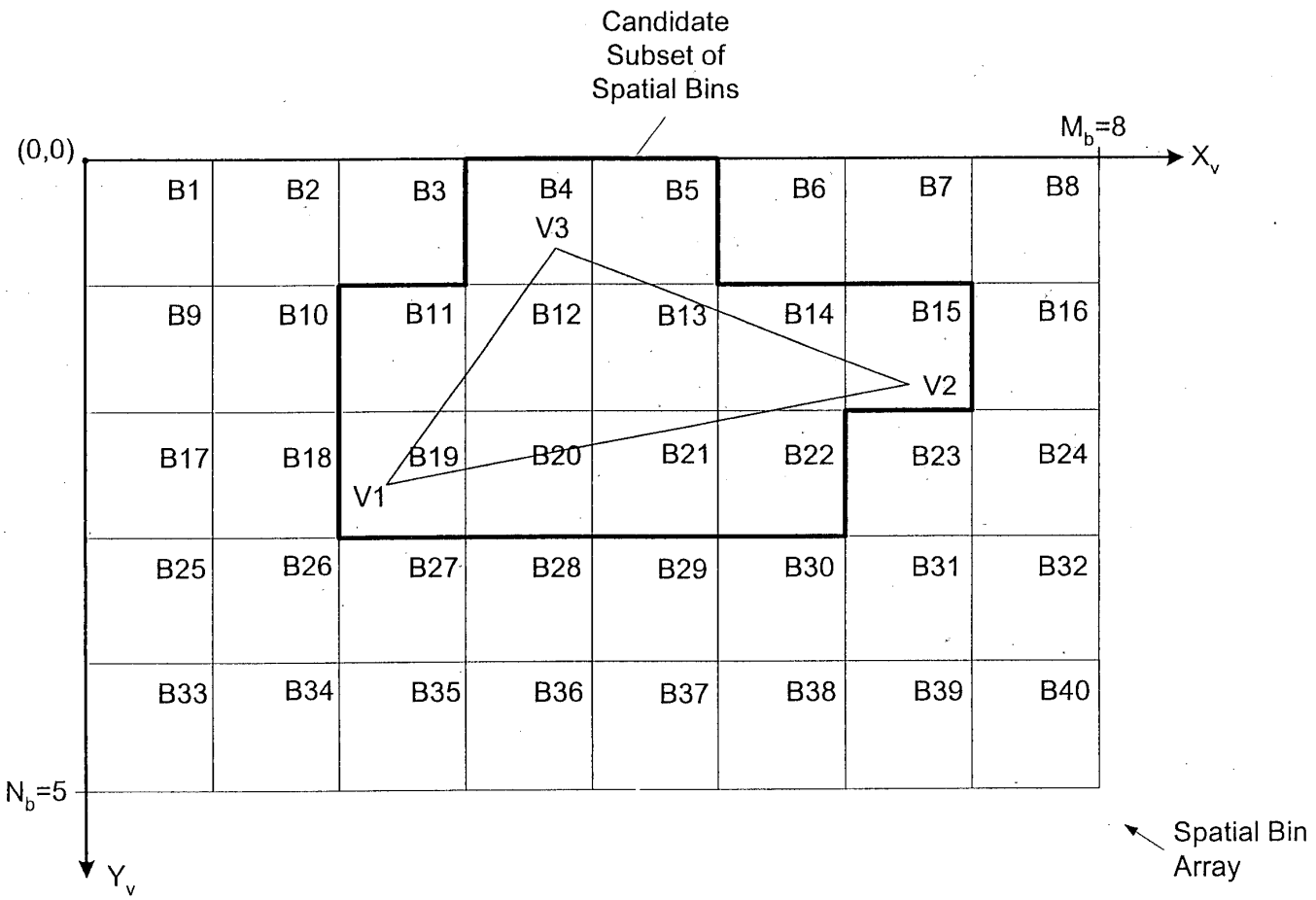

Candidate
Subset of
Spatial Bins
(0,0)
M_b=8
X_v
B1
B2
B3
B4
B5
B6
B7
B8
V3
B9
B10
B11
B12
B13
B14
B15
B16
V2
B17
B18
B19
B20
B21
B22
B23
B24
V1
B25
B26
B27
B28
B29
B30
B31
B32
B33
B34
B35
B36
B37
B38
B39
B40
N_b=5
Y_v
Spatial Bin
Array

Fig. 5

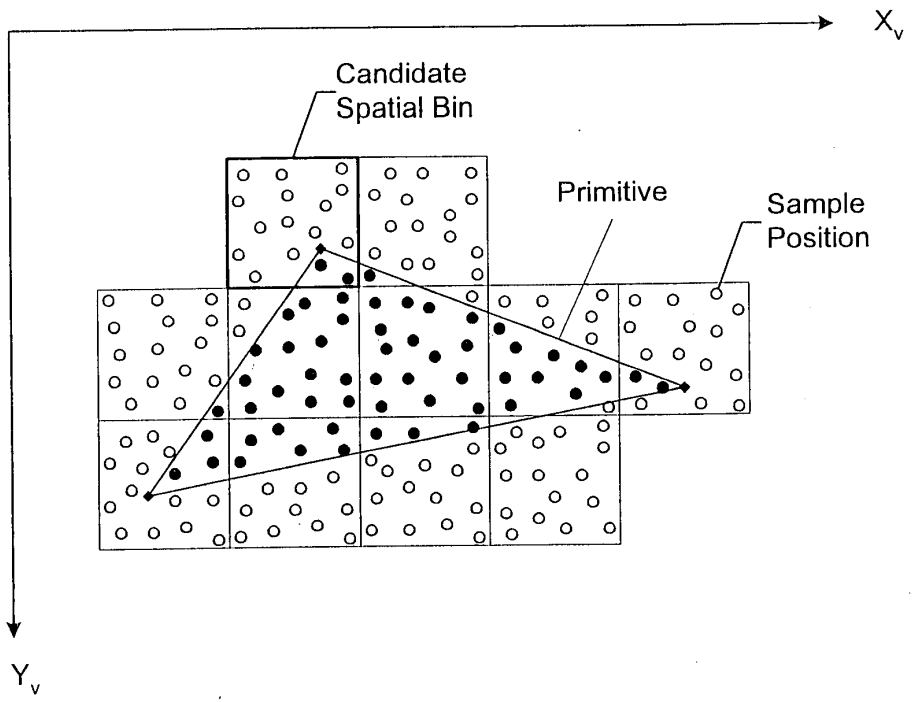


Fig. 6

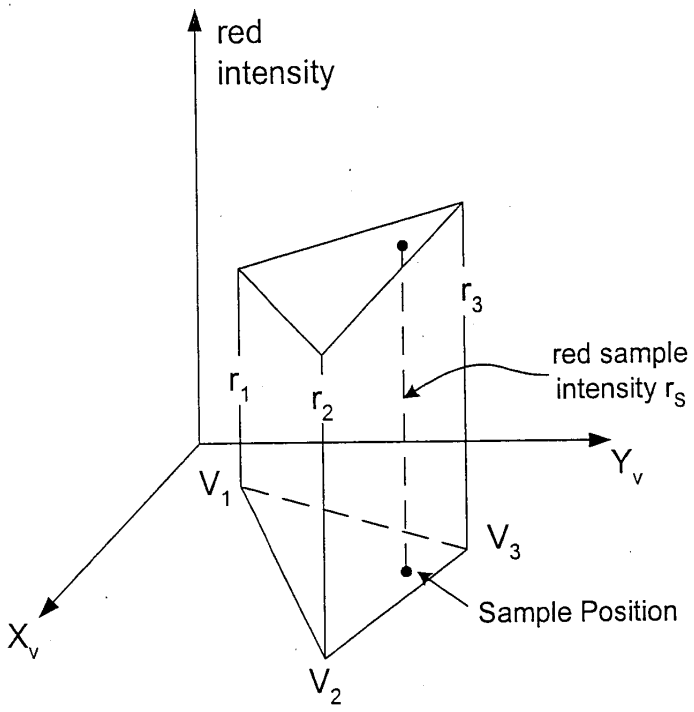

red
intensity
r3
red sample
intensity rS
r1
r2
Yv
V1
V3
Sample Position
Xv
V2

Fig. 7

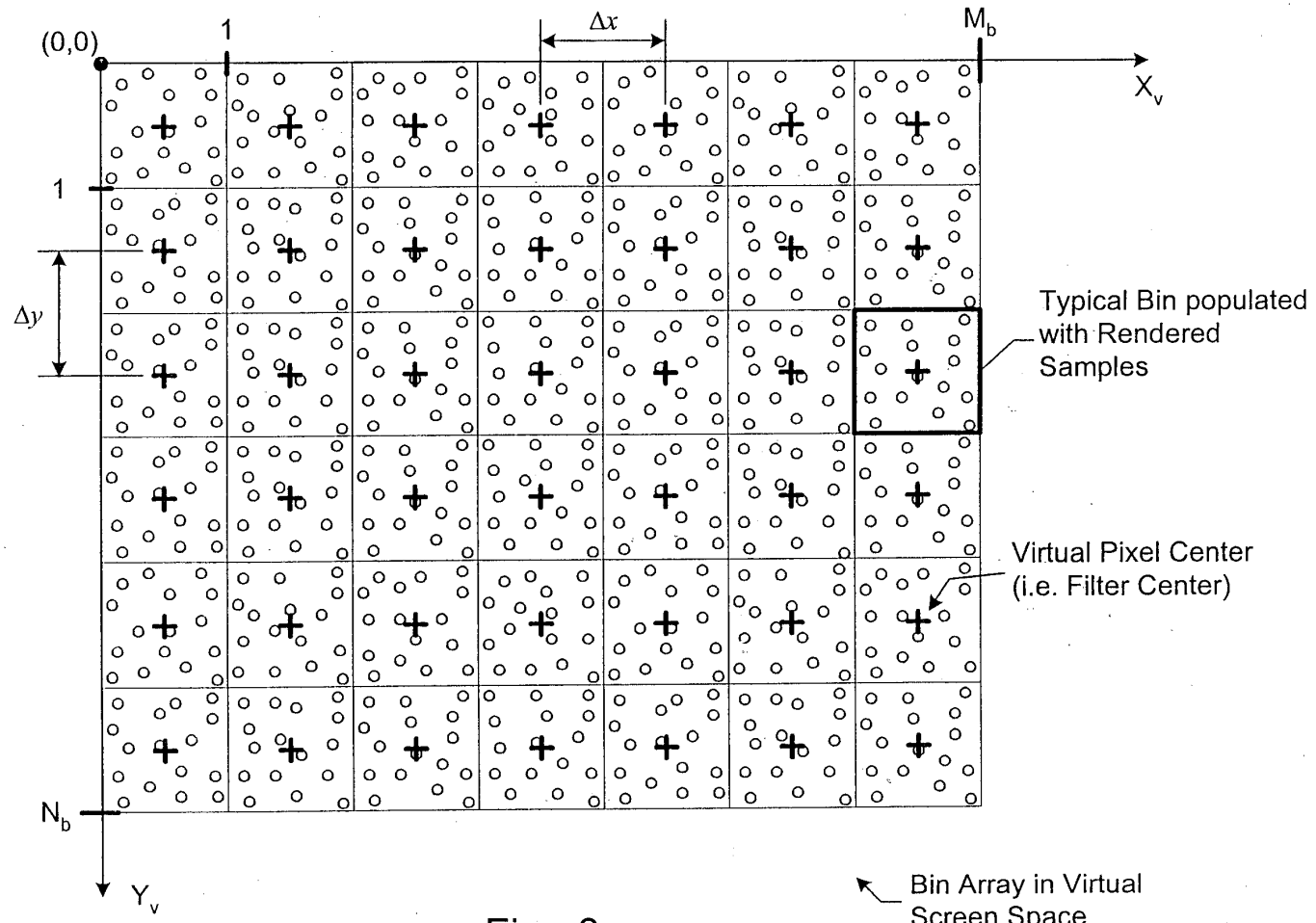

(0,0)
1
Δx
M_b
X_v
1
Δy
Typical Bin populated with Rendered Samples
Virtual Pixel Center (i.e. Filter Center)
N_b
Y_v
Bin Array in Virtual Screen Space

Fig. 8

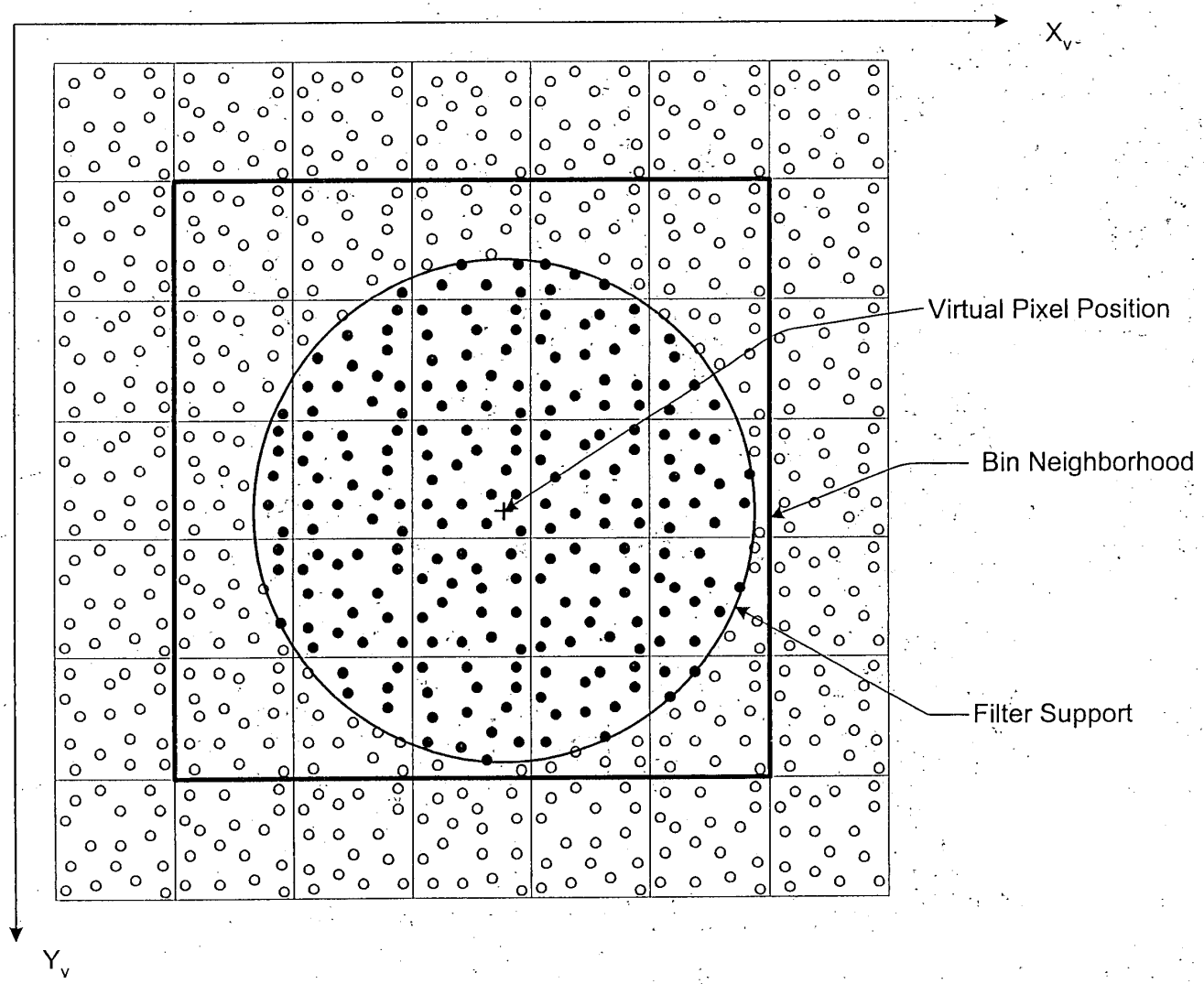

X_v
Y_v
Virtual Pixel Position
Bin Neighborhood
Filter Support

Fig. 9

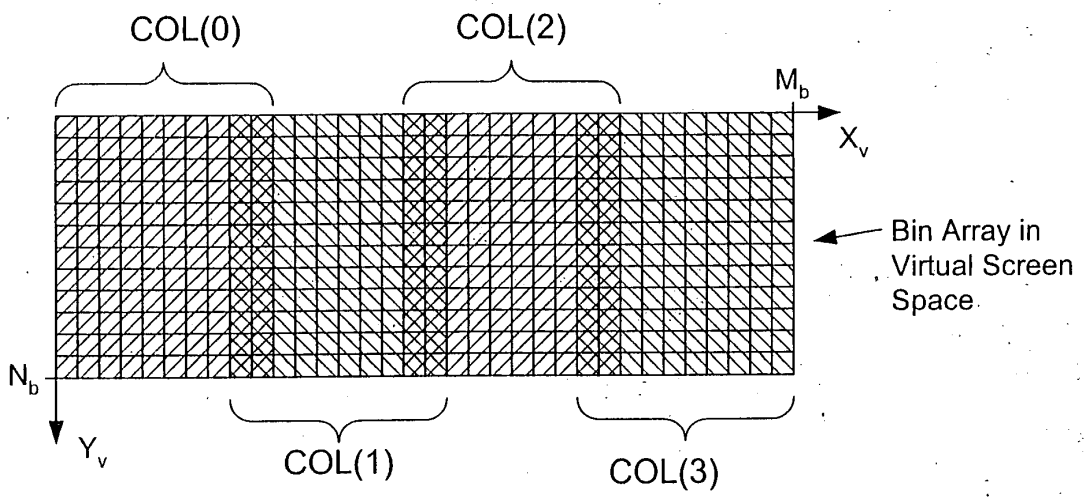

COL(0)
COL(2)
M_b
X_v
Bin Array in Virtual Screen Space
N_b
Y_v
COL(1)
COL(3)

FIG. 10

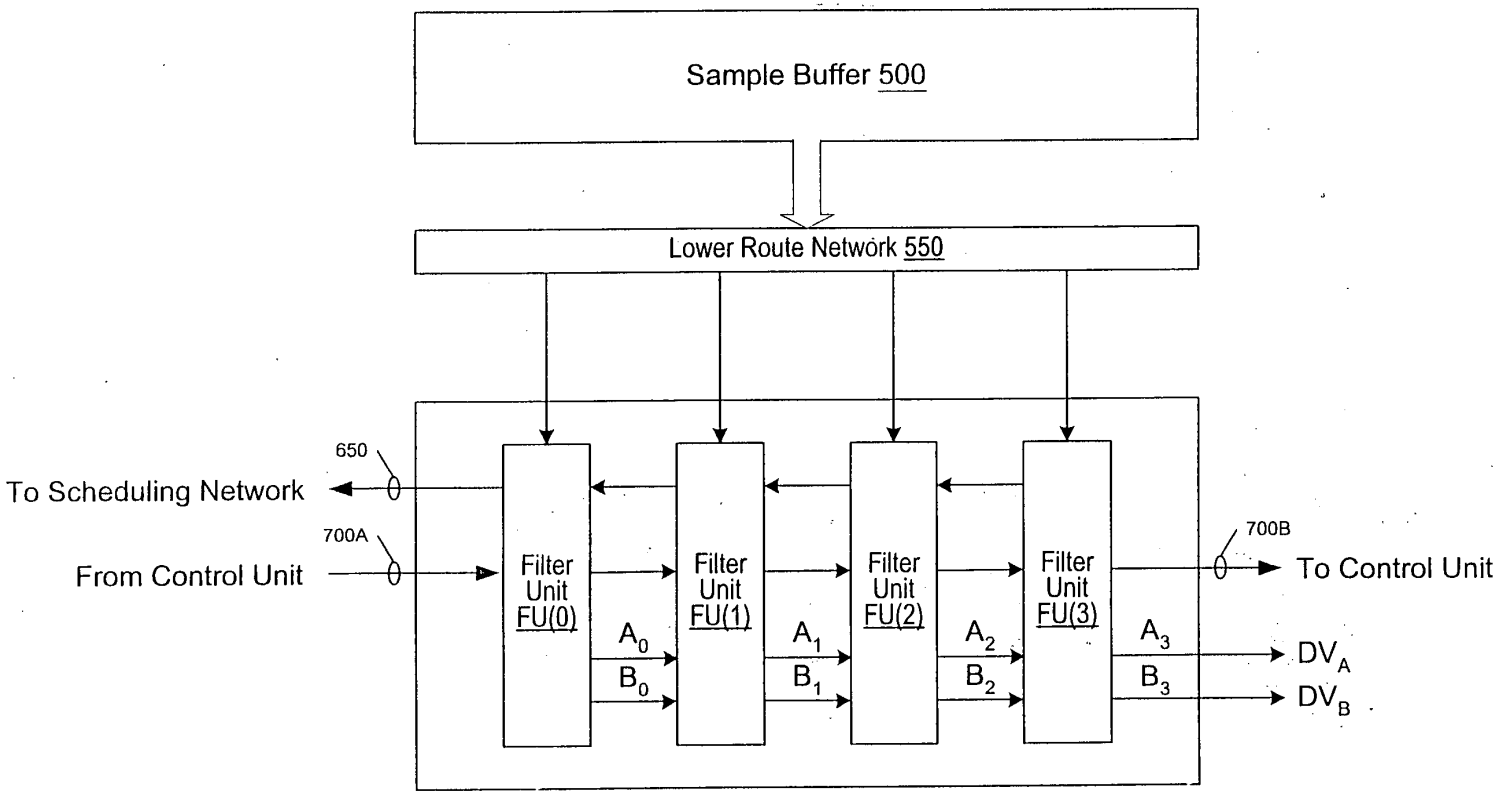

Sample Buffer 500
Lower Route Network 550
650
To Scheduling Network
700A
From Control Unit
Filter Unit FU(0)
Filter Unit FU(1)
Filter Unit FU(2)
Filter Unit FU(3)
A0
B0
A1
B1
A2
B2
A3
B3
700B
To Control Unit
DVA
DVB

FIG. 11

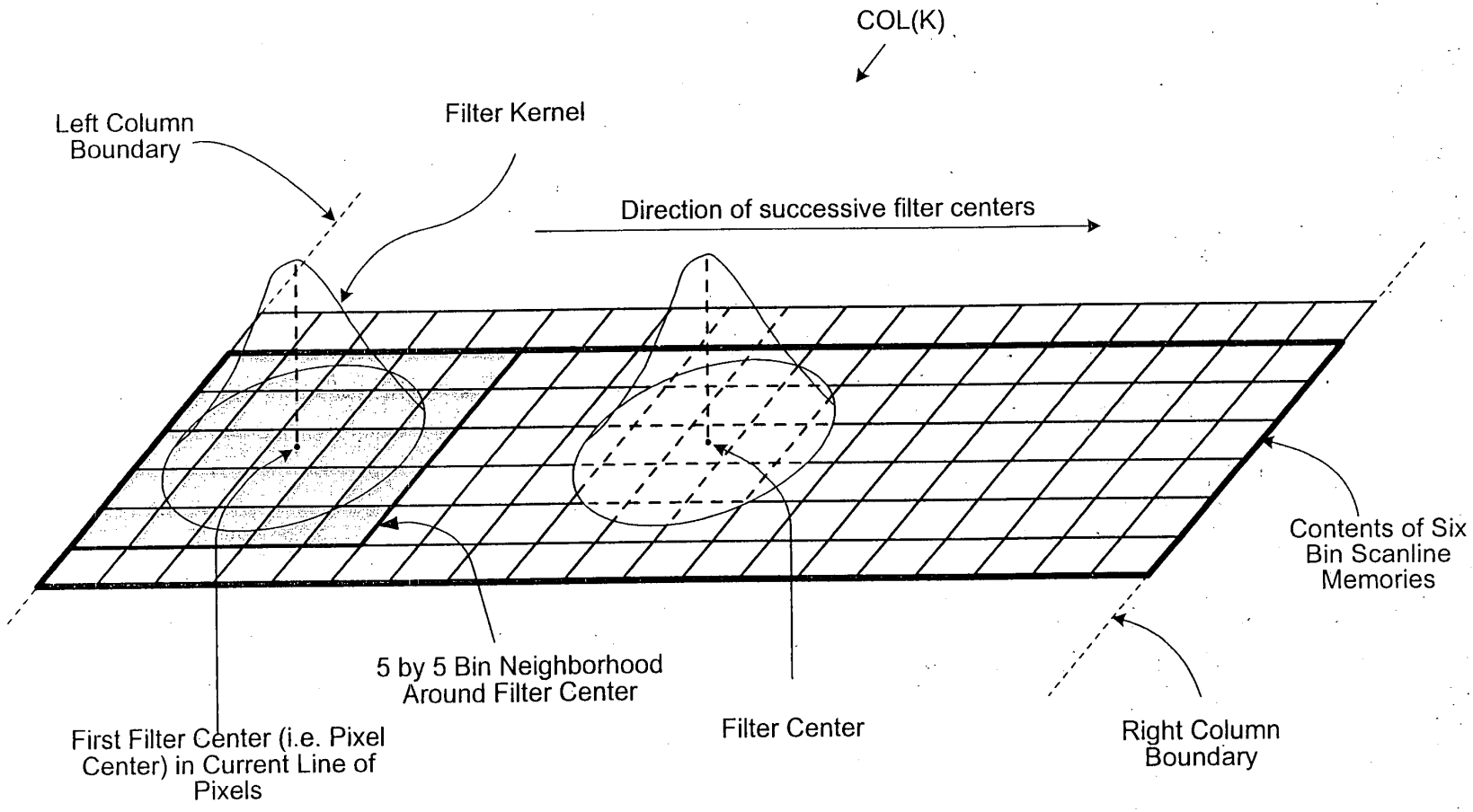

COL(K)
Left Column Boundary
Filter Kernel
Direction of successive filter centers
Contents of Six Bin Scanline Memories
5 by 5 Bin Neighborhood Around Filter Center
First Filter Center (i.e. Pixel Center) in Current Line of Pixels
Filter Center
Right Column Boundary

FIG. 12

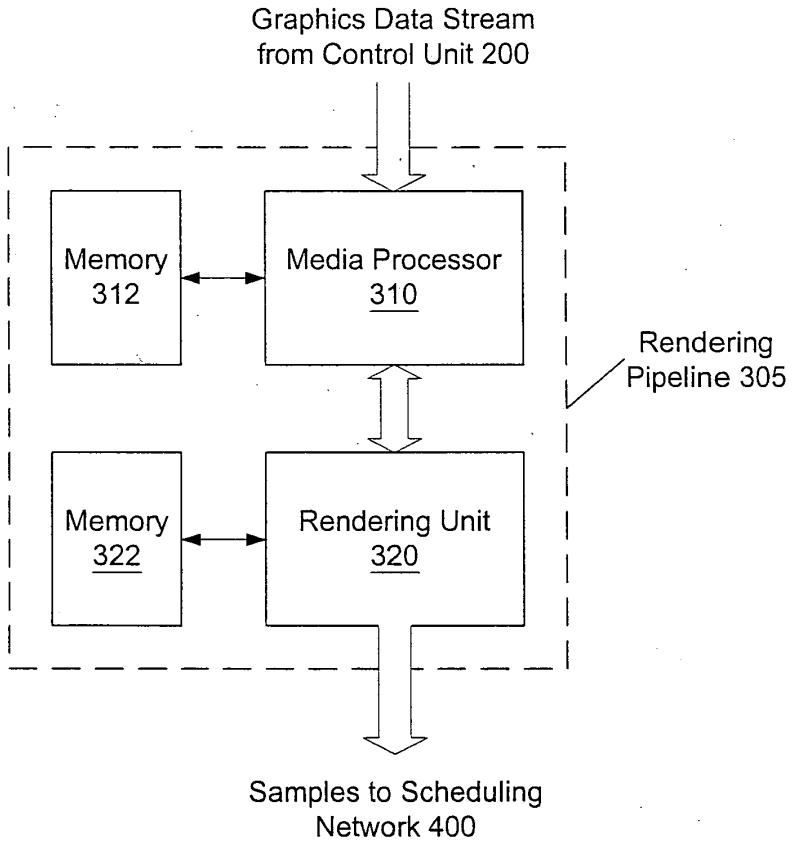

Graphics Data Stream
from Control Unit 200
Memory
312
Media Processor
310
Rendering
Pipeline 305
Memory
322
Rendering Unit
320
Samples to Scheduling
Network 400

Fig. 13

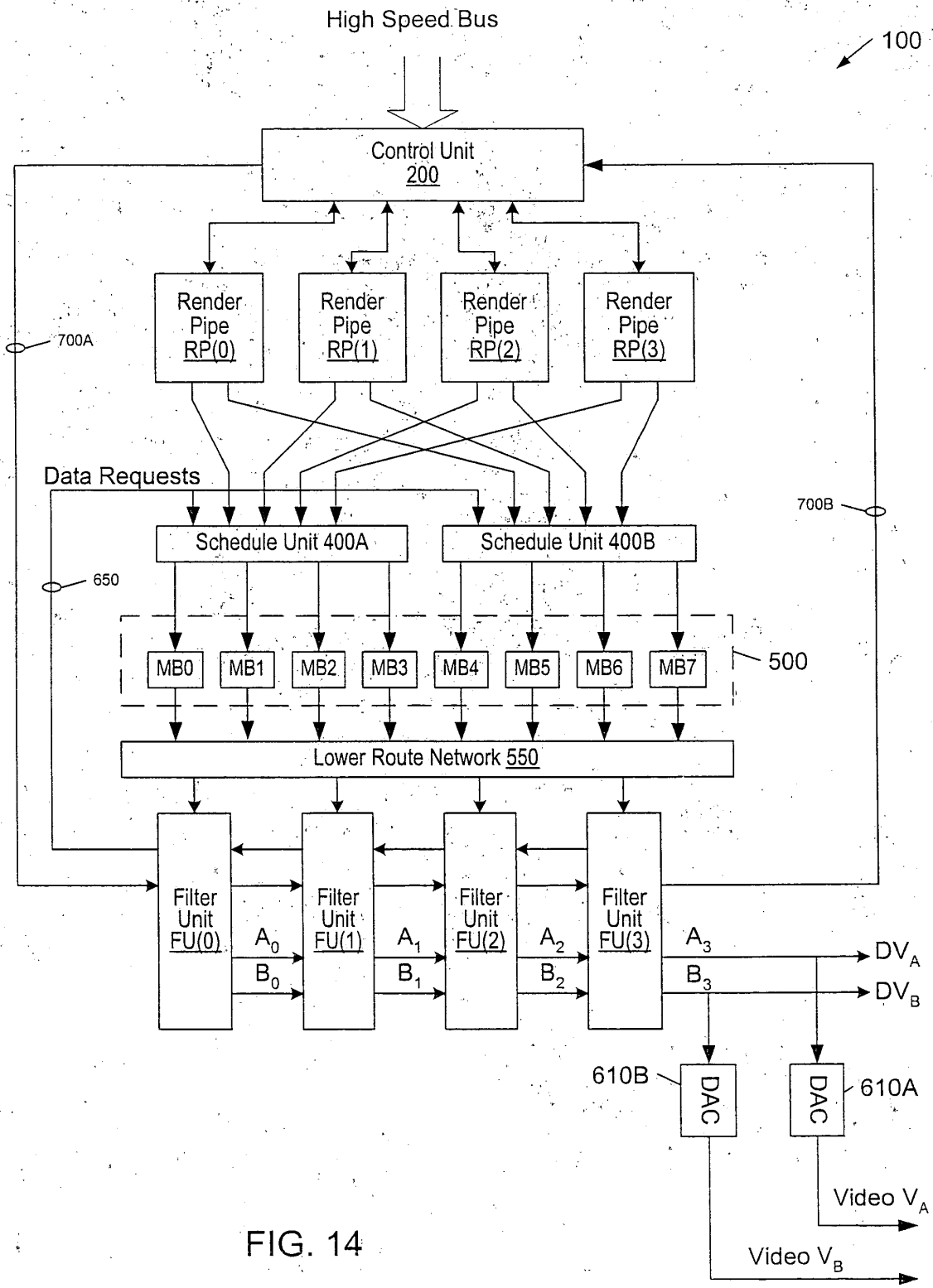

High Speed Bus
100
Control Unit
200
Render Pipe RP(0)
Render Pipe RP(1)
Render Pipe RP(2)
Render Pipe RP(3)
700A
Data Requests
700B
Schedule Unit 400A
Schedule Unit 400B
650
MB0
MB1
MB2
MB3
MB4
MB5
MB6
MB7
500
Lower Route Network 550
Filter Unit FU(0)
Filter Unit FU(1)
Filter Unit FU(2)
Filter Unit FU(3)
A0
B0
A1
B1
A2
B2
A3
B3
DVA
DVB
610B
DAC
DAC
610A
Video VA
Video VB

FIG. 14

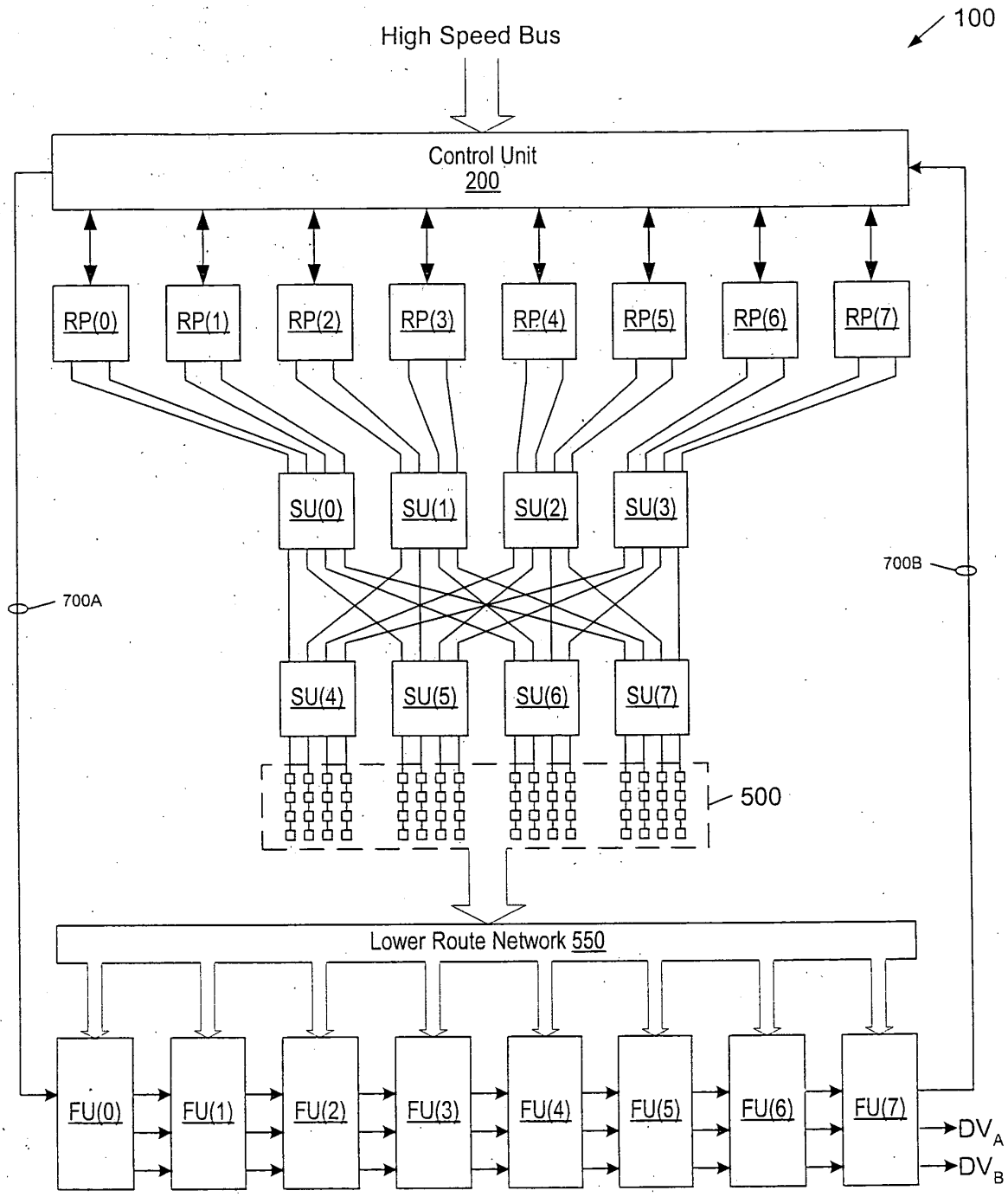

100
High Speed Bus
Control Unit
200
RP(0)
RP(1)
RP(2)
RP(3)
RP(4)
RP(5)
RP(6)
RP(7)
SU(0)
SU(1)
SU(2)
SU(3)
SU(4)
SU(5)
SU(6)
SU(7)
700A
700B
500
Lower Route Network 550
FU(0)
FU(1)
FU(2)
FU(3)
FU(4)
FU(5)
FU(6)
FU(7)
DV_A
DV_B

Fig. 15

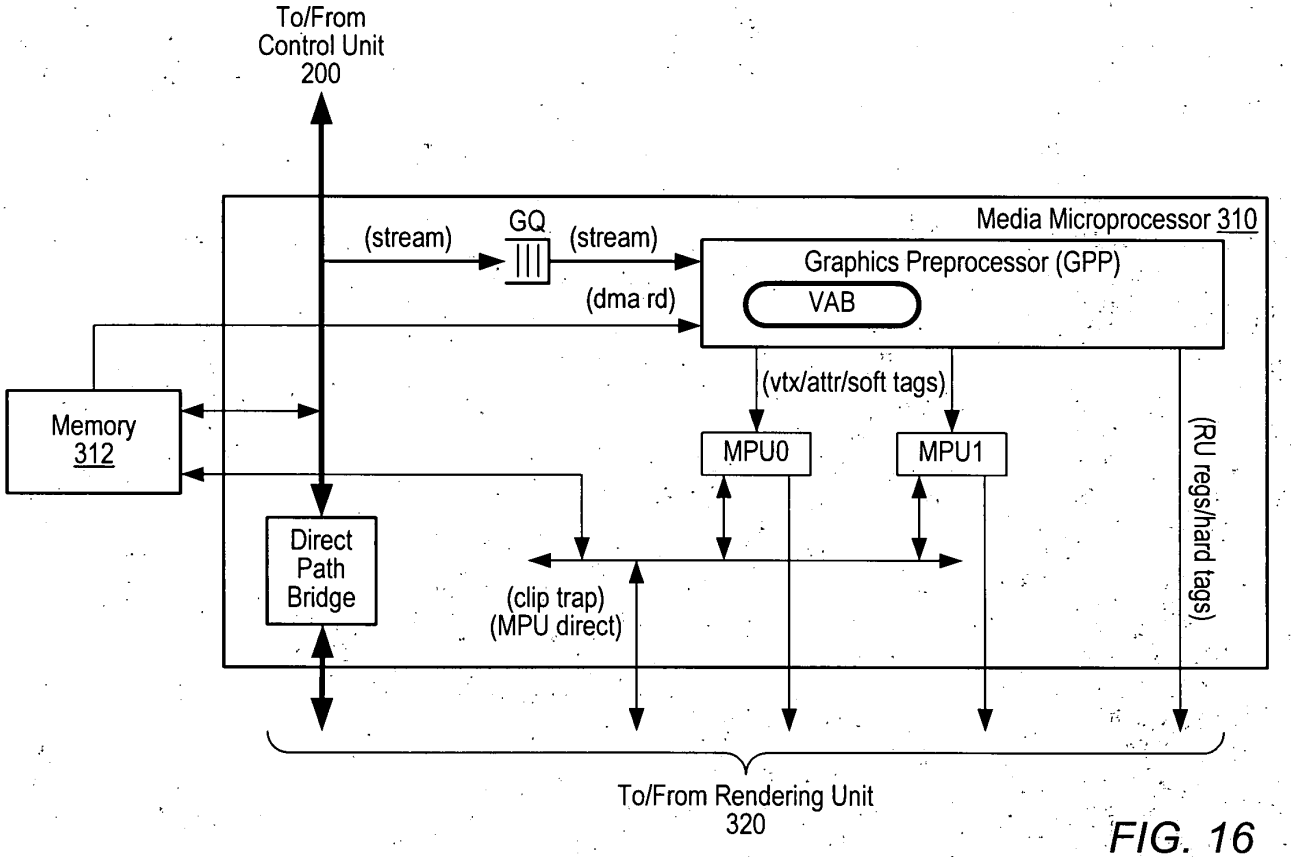

To/From
Control Unit
200
Media Microprocessor 310
(stream)
GQ
(stream)
Graphics Preprocessor (GPP)
VAB
(dma rd)
(vtx/attr/soft tags)
Memory
312
MPU0
MPU1
(RU regs/hard tags)
Direct
Path
Bridge
(clip trap)
(MPU direct)
To/From Rendering Unit
320

FIG. 16

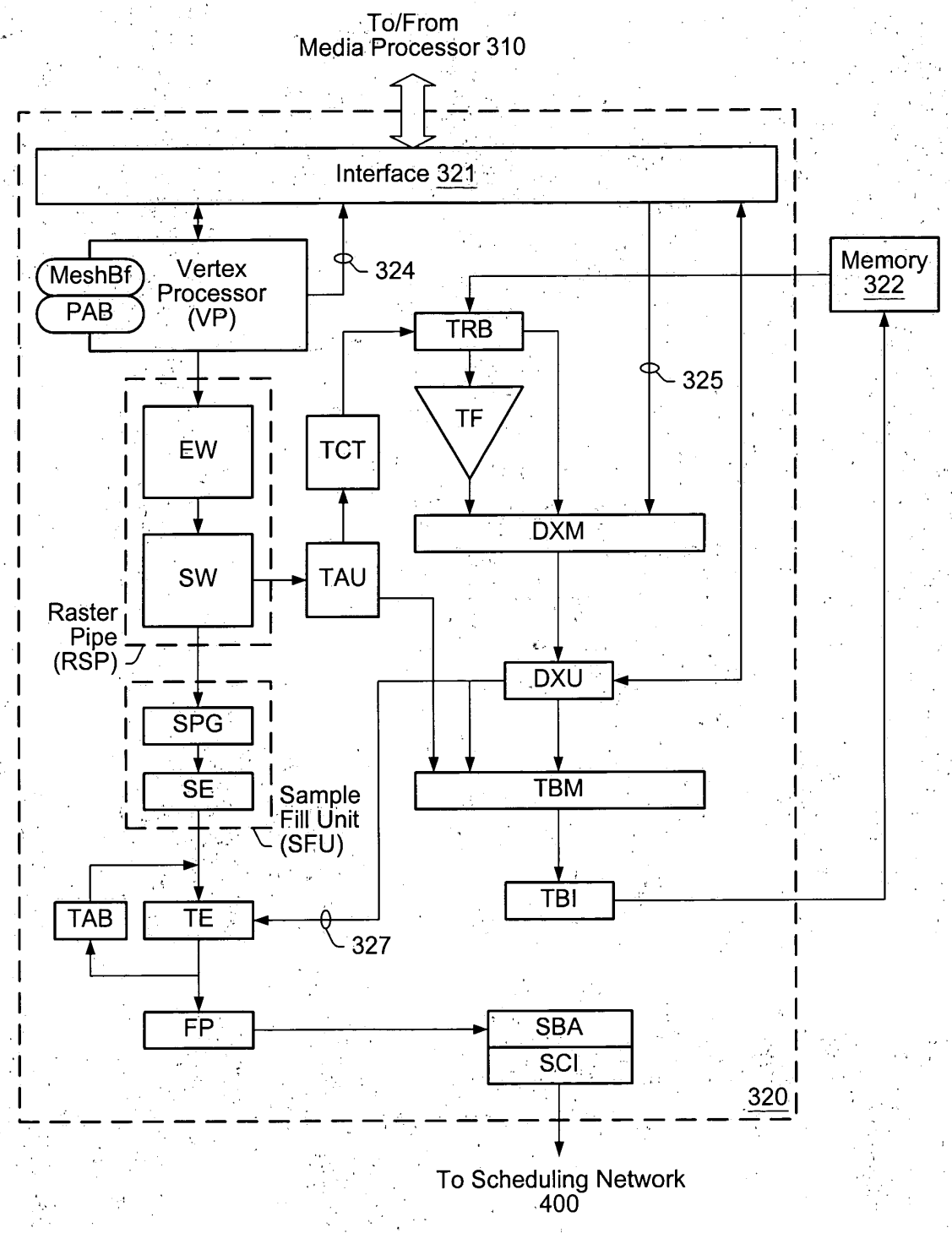

To/From
Media Processor 310
Interface 321
MeshBf
PAB
Vertex
Processor
(VP)
324
Memory
322
TRB
325
TF
EW
TCT
DXM
SW
TAU
Raster
Pipe
(RSP)
DXU
SPG
SE
Sample
Fill Unit
(SFU)
TBM
TBI
TAB
TE
327
FP
SBA
SCI
320
To Scheduling Network
400

Fig. 17

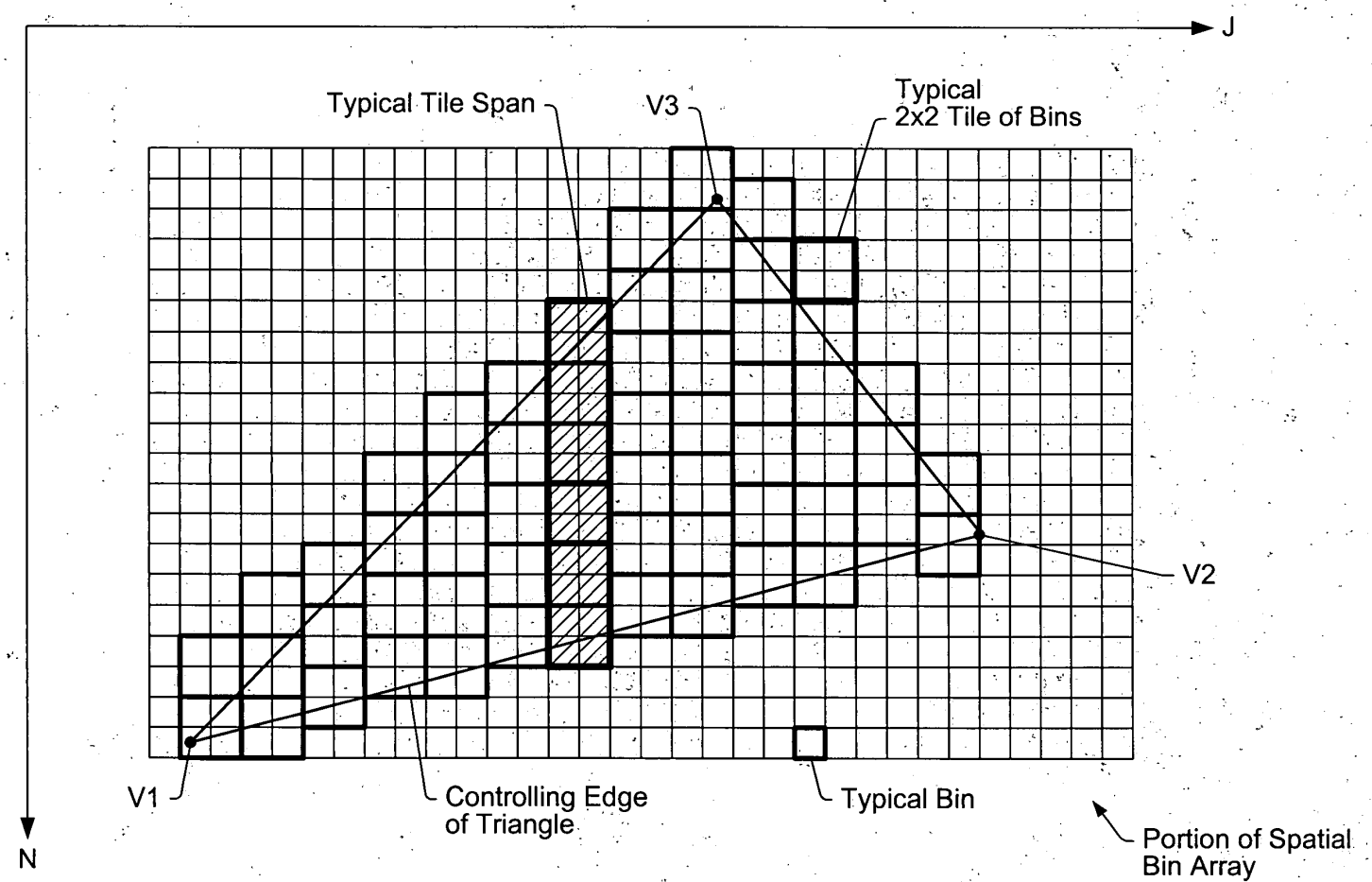

J
N
Typical Tile Span
V3
Typical
2x2 Tile of Bins
V2
V1
Controlling Edge
of Triangle
Typical Bin
Portion of Spatial
Bin Array

Fig. 18

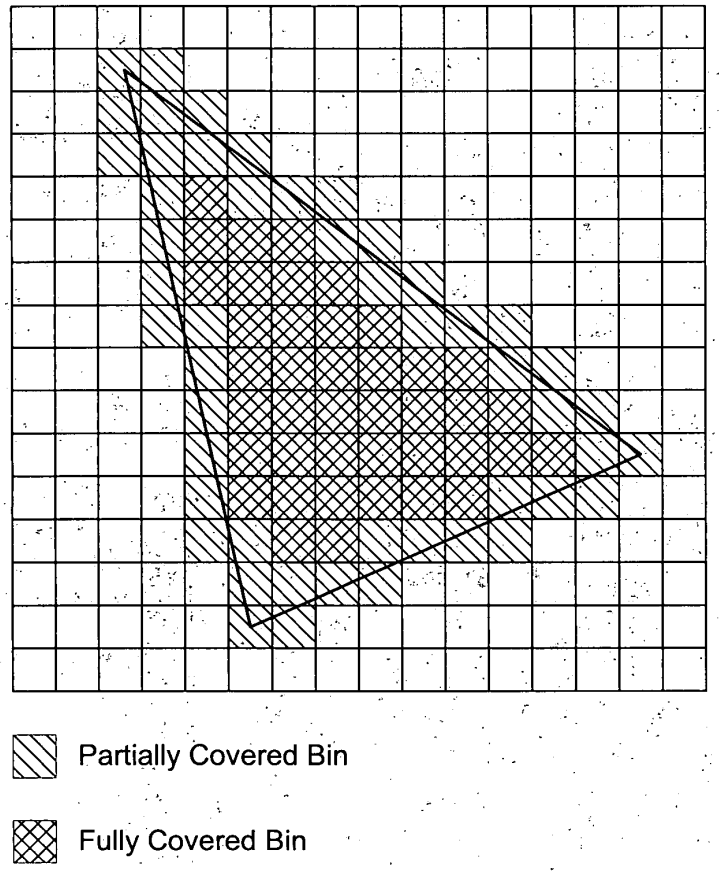

Partially Covered Bin
Fully Covered Bin

Fig. 19

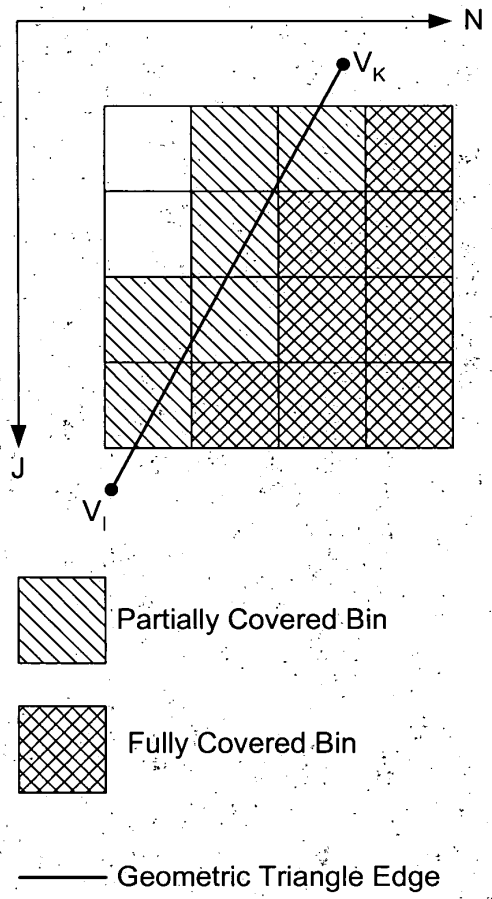

N
J
V_K
V_I
Partially Covered Bin
Fully Covered Bin
Geometric Triangle Edge

Fig. 20

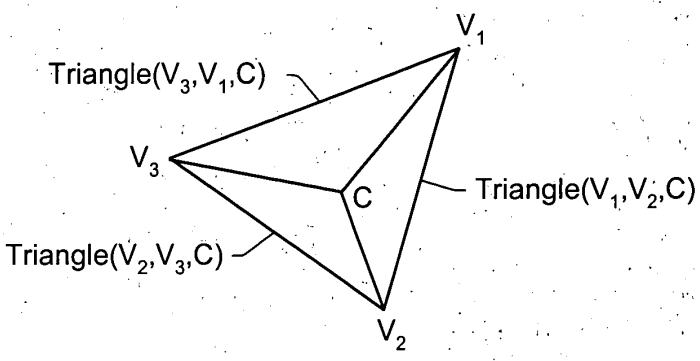

V1
Triangle(V3,V1,C)
V3
C
Triangle(V1,V2,C)
Triangle(V2,V3,C)
V2

Fig. 21

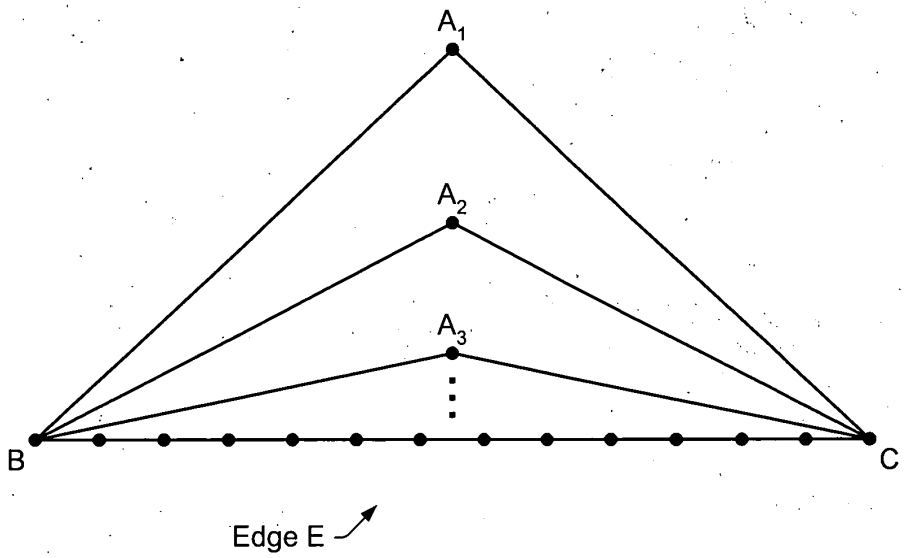

A1
A2
A3
B
C
Edge E

Fig. 22

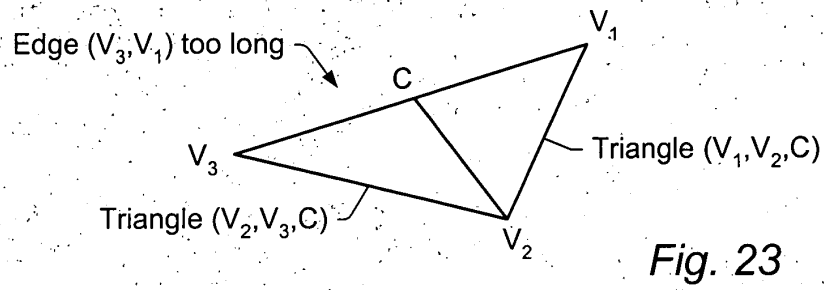


Fig. 23

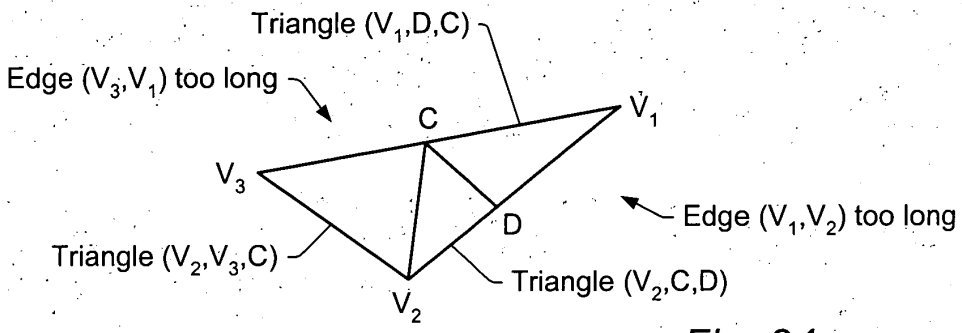


Fig. 24

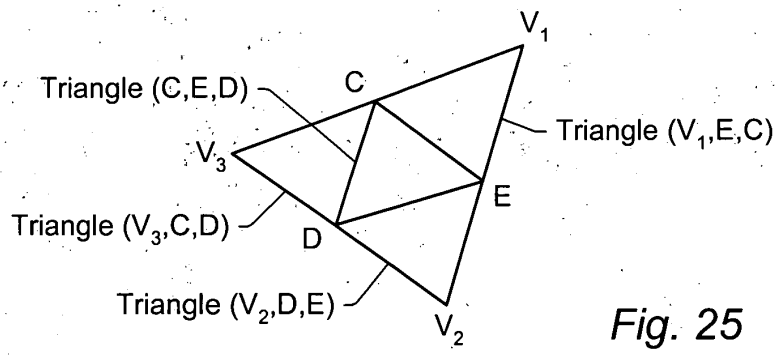


Fig. 25

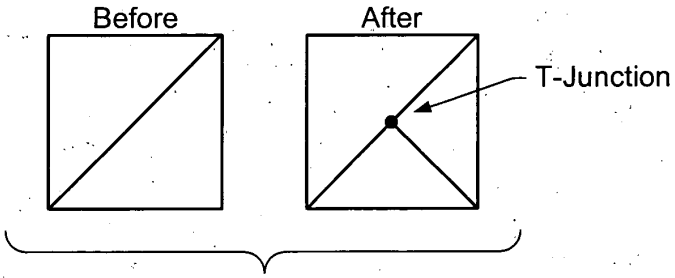


Fig. 26

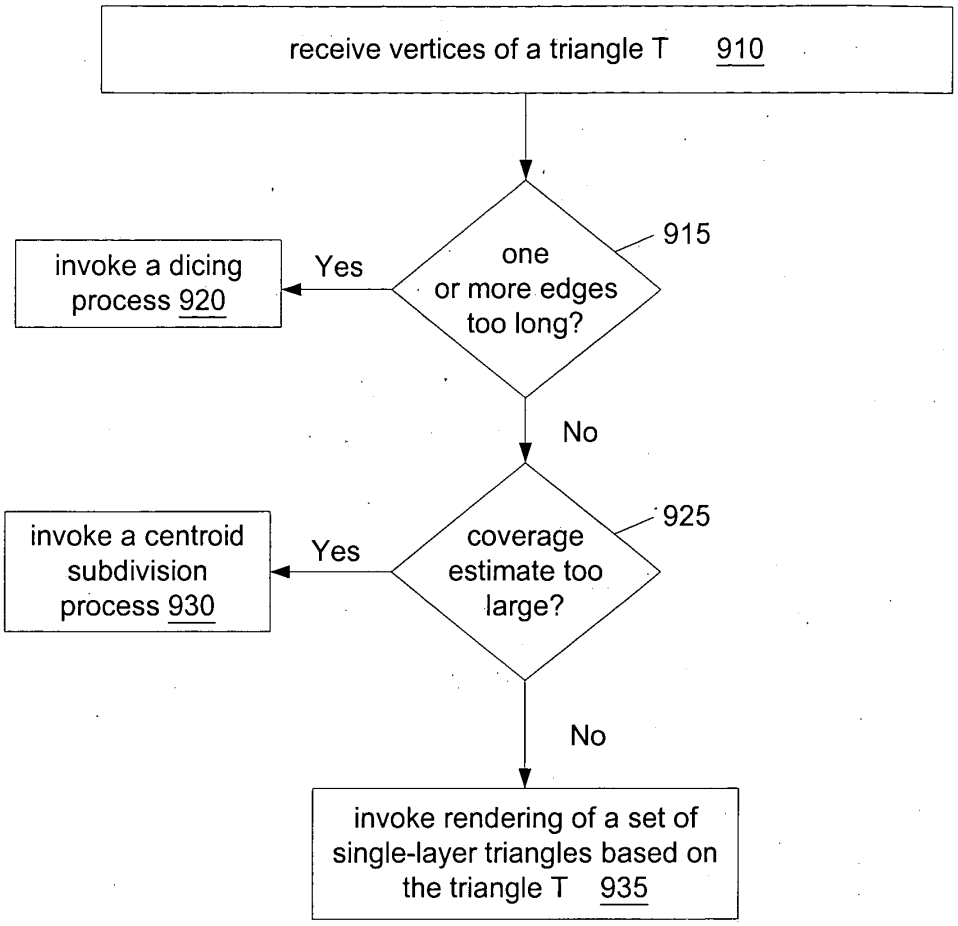

receive vertices of a triangle T 910
one or more edges too long?
915
Yes
invoke a dicing process 920
No
coverage estimate too large?
925
Yes
invoke a centroid subdivision process 930
No
invoke rendering of a set of single-layer triangles based on the triangle T 935

Fig. 27